Create Hierarchical and Multiple Page Designs with “gEDA”

HOWTO/ Wish List / White Paper

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Version 1.1 Added: Multiple page flat designs by: Peter Kaiser	27. Jan. 04
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Table of Contents

1. Hierarchical Designs

1.1 Upper level

Create a symbol somewhere along the “component-library” search path, defined in gschemrc. The name of the symbol should be the same as the name of the lower level schematic, but with the extension “*.sym”: <lower_level_schematic_name.sym>

Place the following attribute on the symbol:

source=<lower_level_schematic_name.sch>, visible or invisible
refdes=X?, visible

Attach the the following attributes to each pin of the symbol:

pinlable=<signal_name>, visible
pinnumber=1, 2, IN, Out, ...; comment only
pinseq=1, 2. ...; invisible, comment only

Place the symbol in the upper level schematic.

Opens:
- Pinnumber and pinlable may have the same value. Both are visible? Can one reference to the other.

1.2 Lower level

Create a new schematic called <lower_level_schematic_name.sch>. This must be in the somewhere in the “source-library” search path defined in gschemrc. Example definition:

(source-library “.”)

Use the symbol “in-1” or “out-1” form the library “IO”, connect it to a net. Change the value of the refdes attribute to <signal_name>. The signal name must be the same as the pinlable attribute on the previous crated symbol.

Alternatively you can create your own symbol. The symbol needs one pin with the following attributes:

refdes=<signal_name>; visible

optional:
device=input, output, ...; invisible.

pin attributes:
pinnumber=1; invisible
pinseq=1; invisible

Attention: When you use GND and VDD symbols with the “net” attribute, the nets are not connected over the hierarchies!

1.3 Netlist extraction

make sure that you use the same search path in gnetlistrc than in gschemrc. Then use gnetlist in your usual way. To get more information about what gnetlist is doing use the “-v” option.

1.4 Spice Subcircuit

In analog design it is a usual way to create spice subcircuits and connect it to the final netlist on top level. Stuarts “spice-sdb” did a pretty good job on this. For information how to do this look at www.brorson.com/gEDA/SPICE/netlist.html#hierarchy

Opens: How is it possible to use the same connect symbols on the lower level for spice and hierarchal design?

1.5 Verilog Module

With Verilog, you may need the same circuit for different purposes. Netlist for simulation, place and route or test pattern generation. Therefor it is possible to crate a module, that later can be inserted to the new environment. For more information look at the Verilog readme.

2. Multiple Page flat Designs

2.1 Drawing Schematics

Draw the schematic in the usual way and save it:

< schematic_1.sch >
< schematic_2.sch >
< schematic_x.sch > ....

To make a connection between two pages, give the wires the same “netname” attribute.

Buses go over different pages without any problem, because the netname attribute from the net is the only reason for connecting the nets.

Attention: Having the same refdes attribute on different pages leads in fancy error messages.

2.2 Netlist extraction

Use gnetlist in the following way:

```
gnetlist -g <your-netlist>   schematic_1.sch   schematic_2.sch   schematic_x.sch   ....
```

or use wildcards:

```
gnetlist -g <your-netlist>   schematic_?.sch
```

Good luck and have fun.

10. Wish List / To Do

- Create testbench in “netlist_test” for spice-sdb.

- How can I define global signals in hierarchal designs.
    With the net=gnd! attribute?
    Without any attribute ?

- Script for automatic creation of:
    Symbols from the lower level schematic, test gnetman.
    Placed ports from the upper level schematic.

- Different views for a lower level circuit. For example:
    - Transistor view
    - Behavioral view
    - Verilog view
    - Subcircuit definition only, for Spice

- Buses don't go over hierarchal designs with gnetlist, but with gnetman. Test of gnetman